Notice of References Cited	Application/Control No. 09/591,621	Applicant(s)/Patent Under Reexamination GUPTA, VIDYABHUSAN	
	Examiner Morella I Rosales-Hanner	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,604,067 B1	08-2003	Abraham et al.	703/21
	B	US-6,263,302 B1	07-2001	Hellestrand et al.	703/17
	C	US-6,052,524	04-2000	Mark R. Pauna	395/500.43
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	T Vinod Kumar Gupta & Purvesh Sharma. "Processor Evaluation in an Embedded Systems Design Environment B. Tech Project." May 1999 Deparment of Computer Science & Engineering Indian Institute of Technology, Delhi
	V	T.V.K. Gupta, Purvesh Sharma, M. Balakrishnan & Sharad Malik. "Professor Evaluation in an Embedded Systems Design Environment.", Jan 2000, VLSI Design 2000, 13th Annual International Conference
	W	Barry Shackleford , Mitsuhiro Yasuda, Etsuko Okushi , Hisao Koizumi, Hiroyuki Tomiyama & Hiroto Yasuura. "Memory-CPU size optimization for embedded system designs. " 1997 Annual ACM IEEE Design Automation Conference.
	X	J. Takala, M. Kuulusa, P. Ojala & J. Nurmi. "Enhanced DSP core for embedded applications." Signal Processing Systems, 1999. SiPS 99. 1999 IEEE Workshop on , 20-22 Oct. 1999

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 09/591,621	Applicant(s)/Patent Under Reexamination GUPTA, VIDYABHUSAN	
	Examiner Morella I Rosales-Hanner	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,604,067 B1	08-2003	Abraham et al.	703/21
	B	US-6,263,302 B1	07-2001	Hellestrand et al.	703/17
	C	US-6,052,524	04-2000	Mark R. Pauna	395/500.43
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	T Vinod Kumar Gupta & Purvesh Sharma. "Processor Evaluation in an Embedded Systems Design Environment B. Tech Project." May 1999 Deparment of Computer Science & Engineering Indian Institute of Technology, Delhi
	V	T.V.K. Gupta, Purvesh Sharma, M. Balakrishnan & Sharad Malik. "Professor Evaluation in an Embedded Systems Design Environment.", Jan 2000, VLSI Design 2000, 13th Annual International Conference
	W	Barry Shackleford , Mitsuhiro Yasuda, Etsuko Okushi , Hisao Koizumi, Hiroyuki Tomiyama & Hiroto Yasuura. "Memory-CPU size optimization for embedded system designs. " 1997 Annual ACM IEEE Design Automation Conference.
	X	J. Takala, M. Kuulusa, P. Ojala & J. Nurmi. "Enhanced DSP core for embedded applications." Signal Processing Systems, 1999. SiPS 99. 1999 IEEE Workshop on , 20-22 Oct. 1999

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.